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(54) [Title of the Invention] DRIVING CIRCUIT OF LIQUID CRYSTAL DISPLAY DEVICE

(57) [Abstract]

[Purpose]

To provide a driving circuit having high resolution of a liquid crystal display device, which is simple in structure and inexpensive.

[Constitution]

This driving circuit of a liquid crystal display device is provided with a digital comparator adapted to sequentially store a digital video signal formed of n-bit pixel data in an m-stage n-bit shift register line by line, latch the same by m-stage n-bit latch circuit for one horizontal period to coincide in parallel with n-bit counter output by each stage and lead out a coincidence pulse, analog ramp waveform between a white level and a black level is sampled in the timing of generating the coincidence pulse and fed to a signal line of a TFT array driving the liquid crystal. The analog ramp waveform is corrected according to the gamma control characteristic of liquid crystal.

[Claims]

[Claim 1]

A driving circuit of a liquid crystal display device, in a driving circuit of an active matrix type liquid crystal display device adapted to drive a liquid crystal display device by a matrix array formed of a thin film transistor made of polysilicon, comprising: a shift register circuit for sequentially storing a digital video signal formed of a series of n-bit pixel data for one line each; a latch circuit for latching the digital video signal for one line sequentially stored in the shift register circuit for one horizontal period; a digital comparator circuit for comparing each pixel data constituting the digital video signal for one line output from the latch circuit with a data value output from an n-adic counter and generating a coincidence pulse at the point of time of coincidence; a conversion analog signal generating circuit for generating an analog ramp waveform between a white level and a black level in every horizontal period; and an analog switch circuit for sampling the analog ramp waveform from the converting analog signal generating circuit in response to the coincidence pulse to generate analog voltage of a level corresponding to the timing of generating the coincidence pulse, wherein the sampling output from the analog switch circuit is supplied to a thin film transistor corresponding to a designated pixel in the selected horizontal line of the matrix array, and a designated analog video signal is fed to a designated pixel of the liquid crystal display device.

[Claim 2]

The driving circuit of the liquid crystal display device according to claim 1, wherein the conversion analog signal generating circuit for generating an analog ramp waveform in every horizontal period is provided with a gamma control circuit for performing gamma control on a video signal according to the voltage-transmittance characteristic of liquid crystal to the analog cramp waveform.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Application]

This invention relates to a driving circuit of a liquid crystal display device and particularly to the driving circuit of an active matrix type liquid crystal display device having a thin film transistor matrix array using a polysilicon TFT (hereinafter referred to as TFT array).

[0002]

[Prior Art]

As the driving circuit for driving a horizontal line of a polysilicon active matrix type liquid crystal display device, a circuit shown in Fig. 8, for example, has been proposed heretofore. In Fig. 8, the reference numeral 21 is a shift register, which sequentially generates a sampling pulse by a start pulse 22 and a clock 23 to thereby sequentially turn on an analog switch 24 disposed in a corresponding source line 28 of the liquid crystal display device, and sequentially feeds an analog video signal 25 fed from one side of the analog switch 24 to the source line 28. Each pixel 20 of a liquid crystal display element 27 is charged with the video signal through a thin film transistor (hereinafter referred to as TFT) 30 of a horizontal line 29 selected by a scan side driver 26.

[0003]

On the other hand, the reference numerals 1, 2, 3 are A-D conversion circuits for converting R, G and B signals of input analog video signals to digital signals, and the R, G and B signals converted to the digital signals by the A-D conversion circuits 1, 2, 3 are processed by a digital video signal processing circuit 4. The digital video signals R, G, B processed by the digital video signal processing circuit 4 are respectively converted to analog signals by D-A conversion circuits 5, 6, 7 and then amplified to be fed as the analog video signal 25 to the analog switch 24.

[0004]

In Fig. 8, the illustrated liquid crystal display element 27 is adapted to perform monochromatic display, but the respective source lines are provided corresponding to the R, G and B signals to form a driving circuit of a liquid crystal display device for performing color display.

[0005]

As a circuit for driving the source line of the active matrix type liquid crystal display device using the amorphous silicon TFT, a circuit shown in Fig. 9, for example, has been proposed. This is different from that shown in Fig. 8, in that a video signal is a digital signal, and the circuit is composed of a shift register circuit (a data register) 32 for sequentially storing a digital video signal SVd formed of pixel data with a designated bit for one line each, a latch circuit 33 for latching the digital video signals for one line sequentially stored in the shift register circuit 32 for one horizontal period, a digital comparator circuit 34 for comparing each pixel data constituting the digital video signals for one line output from the latch circuit 33 with a data value sequentially increased or decreased and output from an n-bit counter 39 to generate a coincidence pulse 40 at the point of time of coincidence, an analog switch circuit 36 for sampling converting analog input voltage 41 of a ramp waveform synchronized with one cycle of the n-adic counter 39 normally supplied from the outside in response to the coincidence pulse 40, an analog latch circuit 37 for latching the sampling output from the analog switch circuit 36 for the next one horizontal period, and an output stage 38. In the drawing, the reference numeral 271 is a liquid crystal display element in which amorphous silicon TFTs 301 and liquid crystal pixels 201 are arrayed in a matrix.

[0006]

The voltage applied to the liquid crystal and the transmittance of light generally have the relationship as shown by a curve 50 in Fig. 5. When a video signal is applied linearly as it is in the range of the black level and the white level shown in the drawing, the optical output becomes an image contracting near the black and near the white to form an image of lower quality without gradation reproducibility. Therefore, in consideration of the transmittance curve of liquid crystal, an analog video signal and a digital video signal applied to the liquid crystal are previously gamma-controlled according to a video signal correction curve 51 indicated by a dotted line in the drawing.

[0007]

Figs. 10 and 11 are block diagrams of gamma control circuits, in which R, G and B signals of an analog video signal are respectively converted to digital signals by A-D conversion circuits 60, 61, 62, and guided to ROMs 63, 64, 65 for correction, and in the ROMs 63, 64, 65 for correction, the digital R, G and B signals are subjected to gamma control according to look-up table system information depending on the previously stored video signal correction curve 51 shown in Fig. 5.

[0008]

Fig. 10 shows the gamma control circuit adapted to output digital R, G and B signals gamma-controlled in the correction ROMs 63, 64, 65, and Fig. 11 shows the gamma control circuit adapted to convert the digital R, G and B signals to analog R, G and B signals by the D-A conversion circuits 66, 67, 68 and output the same. The digital or analog R, G and B signals are fed to the source line of the liquid crystal display element 27, 271.

[0009]

[Problems that the Invention is to Solve]

The conventional driving circuit shown in Fig. 8 takes a system for directly sampling an analog video signal. Since the driving circuit for driving liquid crystal is formed of polysilicon TFT, the mobility of the transistor is high and the speed is high. Therefore, it may be simple circuit configuration as shown in Fig. 8, but when the number of pixels in the horizontal direction (the number of analog switches, the number of TFTs) is increased to obtain high-resolution display, though it is high speed, the video signal period in one horizontal period is limited so that the time allotted to one sampling is reduced depending on the number of pixels. Further, there is a limitation to charging to high liquid crystal driving voltage because of analog sampling.

[0010]

In order to solve the above problems, an analog video signal has been multiplexed or the time axis has been elongated to increase the number of signals to a liquid crystal driver. These are, however, disadvantageous in that the processing for an external analog video signal is complicated to increase the load of a circuit. On the other hand, in the case where high-grade video processing is desired, digitization is suitable, and as shown in Fig. 8, it is general to go through the process of digitizing an analog video signal by A-D conversion. However, when the device for display takes analog signal input, D-A conversion is required after digital processing, so that the circuit is enlarged for that.

[0011]

On the other hand, in another conventional driving circuit shown in Fig. 9, digital video signal input is taken so that in respect of conversion to an analog signal, there is time to spare to overcome the above disadvantage. This driving circuit, however, has the following disadvantage. That is, since the prior art of Fig. 9 adopts an amorphous silicon TFT operating slowly, an analog signal applied from a source line 28 should give 1H period to the respective sources at the same time so that the output (random in point of time) of an analog switch circuit 36 sampled by the output of a level shifter 35 given to each output line at random is once held, and further applied to the source line 28 through a latch circuit 37 to make all source lines uniform in signal timing and set the hold period to 1H. Thus, after being sampled, again the analog signal is latched and fed to the source line through the buffer, so the circuits are driver IC, resulting in the disadvantage that the chip area is increased for that, and also encountered is the problem that display quality is lowered due to variation of that part.

[0012]

On the other hand, in the driving circuits where look-up type gamma control is performed as shown in Figs. 10 and 11, directly a digital video signal is input to the ROM for correction, so that the conversion time in the ROM should be within one sample. Consequently, the disadvantage is that when a video signal has a small number of pixels in the horizontal direction and a short horizontal period, a high-speed ROM is needed to increase the cost.

[0013]

[Means for Solving the Problems]

The invention has been made to solve the problems of the conventional devices and provide a driving circuit of an active matrix type liquid crystal display device adapted to drive a liquid crystal display device by a matrix array formed of a thin film transistor made of polysilicon, including: a shift register circuit for sequentially storing a digital video signal formed of a series of n-bit pixel data for one line each; a latch circuit for latching the digital video signal for one line sequentially stored in the shift register circuit for one horizontal period; a digital comparator circuit for comparing each pixel data constituting the digital video signal for one line output from the latch circuit with a data value output from an n-adic counter and generating a coincidence pulse at the point of time of coincidence; a converting analog signal generating circuit for generating an analog ramp waveform between a white level and a black level in every horizontal period; and an analog switch circuit for sampling the analog ramp waveform from the conversion analog signal generating circuit in response to the coincidence pulse to generate analog voltage of a level corresponding to the timing of generating the coincidence pulse, wherein the sampling output from the analog switch circuit is supplied to a thin film transistor corresponding to a designated pixel in the selected horizontal line of the matrix array, and a designated analog video signal is fed to a designated pixel of the liquid crystal display device.

[0014]

Further, in the driving circuit of the liquid crystal display device, the conversion analog signal generating circuit for generating an analog ramp waveform in every horizontal period is provided with a gamma control circuit for performing gamma control on a video signal according to the voltage-transmittance characteristic of liquid crystal to the analog ramp waveform.

[0015]

[Operation]

According to the above configuration, the digital video signal formed of a series of n-bit pixel data supplied from the outside is sequentially stored for one line each in the shift register circuit. The digital video signals for one line stored in the shift register circuit are supplied to the latch circuit, and latched here for one horizontal period. Each n-bit pixel data of the digital video signals for one line led out from the latch circuit is compared with the data output from the n-adic counter in the digital comparator circuit to generate a coincidence pulse at a point of time of coincidence at every pixel data.

[0016]

In response to the coincidence pulse generated at every pixel, the analog switch circuit is adapted to sample the analog ramp waveform between the white level and the black level generated in every horizontal period from the conversion analog signal generating circuit to generate analog voltage of a level corresponding to the timing of generating the coincidence pulse, and the analog voltage of each pixel derived from the analog switch circuit is supplied to each corresponding pixel in the horizontal line selected by the scan side driver to make a video display. Since the polysilicon TFT operates fast, short time will be sufficient for the analog signal fed from the source line, so that it is not necessary to hold the output of the analog switch circuit or latch the same.

[0017]

Further, the conversion analog signal generating circuit adapted to generate analog ramp waveform in every horizontal period is provided with the gamma control circuit, whereby the analog ramp waveform is gamma-controlled according to the voltage and transmittance characteristic of liquid crystal. When the thus gamma-controlled analog ramp waveform is supplied to the analog switch circuit, the analog voltage supplied to each pixel is gamma-controlled so that an image without distortion can be reproduced even near the white level and near the black level in the liquid crystal display device.

[0018]

[Embodiments]

Fig. 1 is a block diagram of one embodiment according to the invention. In Fig. 1, the reference numeral 11 is a timing generating circuit, and a horizontal synchronous signal H_D and a vertical synchronous signal V_D synchronized with a digital video signal SVd formed of n-bit data are supplied as a reference timing signal to the timing generating circuit 11. The reference numeral 12 is an m- stage n-bit shift register circuit, and the above n-bit digital video signal SVd is supplied to the shift register circuit 12. A clock CLK is also supplied from the timing generating circuit 11 to the shift register circuit 12, and in each horizontal period, the digital video signal SVd is sequentially stored for one line each.

[0019]

The pixel data for one line stored in the shift register circuit 12 in each horizontal period is supplied to an m-stage n-bit data latch circuit 13. A latch pulse P_L generated within a horizontal blanking period from the timing generating circuit 11 is supplied to the data latch circuit 13, whereby the pixel data for one line supplied from the shift register circuit 12 is latched and held for the next horizontal period. The pixel data for one line outputted from the data latch circuit 13 is supplied to an m-stage n-bit digital comparator circuit 14.

[0020]

On the other hand, a clock CCLK for comparison counter supplied to an n-bit counter 15 and a start pulse Sp outputted in every horizontal period are output from the timing generating circuit 11. In the n-bit counter circuit 15, the outputs QD_0 to QD_n are increased bit by bit in the clock cycle of the clock CCLK for comparison counter in every horizontal period. The outputs QD_0 to QD_n of the n-bit counter circuit 15 are supplied to the m- stage n-bit digital comparator circuit 14.

[0021]

In the digital comparator circuit 14, the pixel data for one line supplied from the data latch circuit 13 and the outputs

QD_0 to QD_n of the n-bit counter circuit 15 are compared by each bit at every stage, and at a point of time of coincidence, a pulse for one clock CCLK for the comparison counter is generated. Each pixel data is n-bit, and the output of the n-bit counter circuit 15 is also n-bit, so within one period of the n-bit counter circuit 15, that is, one horizontal period, all of pixel data for one line can be compared and at a point of time corresponding to the value of the pixel data, a coincidence pulse Cp is output at every stage.

[0022]

Figs. 2 and 3 respectively illustrate a 4-bit configuration circuit as examples of detailed circuit configurations of the m- stage n-bit shift register circuit 12, the data latch circuit 13, the digital comparator circuit 14 and the n-bit counter circuit 15. In the drawings, the parts corresponding to those of Fig. 1 are designated by the same reference numerals. The individual circuit configurations in the respective circuits 12 to 15 are generally used widely, so the detailed description of operation is omitted.

[0023]

On the other hand, the level of the coincidence pulse Cp from the digital comparator circuit 14 is raised to a regulated pulse voltage by a level shifter 16, and supplied to a gate of the subsequent stage analog switch circuit 17. The input of the analog switch circuit 17 is connected to an analog input signal Ta for conversion. The analog input signal Ta for conversion is a ramp waveform from a conversion analog signal generating circuit 18 synchronized with the clock CCLK for the comparison counter from the timing generating circuit 11 in response to the start pulse Sp, and the details are mentioned later.

[0024]

The analog switch circuits 17 at the respective stages are turned on in the period when the coincidence pulse Cp is supplied from the level shifter 16, so that the analog input signal Ta is sampled and the voltage value thereof is a voltage value corresponding to the pixel data. The output of the analog switch circuit 17 at each stage is directly supplied to the source line 28 at each stage corresponding to the TFT matrix array for driving the liquid crystal, thereby charging the liquid crystal of a pixel 20 through a TFT 30 of each stage corresponding to one horizontal line selected to turn on by a scan side driver 26 controlled according to a control signal from the timing generating circuit 11.

[0025]

The period of time when the analog switch circuits 17 at the respective stages turn on is the period of the coincidence pulse Cp of each stage as described above, and this is a long period enough for the pixel clock so that an image can be written stably. That is, in the case where the image effective period of one horizontal period is taken as T_H, supposing that the number of pixels in the horizontal direction is 1000, the period of $T_H/1000$ is the period of the pixel clock and the sampling period of the analog switch circuit 17 in the conventional configuration shown in Fig. 8. However, in the case where the pixel data is 8 bits in the configuration of the invention shown in Fig. 1, even in the case of 1000 pixels, the period is $T_H/256$ so that the time about four times as much as before can be taken.

[0026]

Fig. 4 is a diagram showing the signal conversion process to the time axis in the case of leading out a coincidence pulse Cp from the m- stage n-bit digital comparator circuit 14 by the n-bit counter circuit 15, and obtaining source line output by the level shifter 16, the analog switch circuit 17 and the conversion analog signal generating circuit 18, which illustrates the case of a 4-bit signal at the L- th stage.

[0027]

In Fig. 4, (a) shows a counter output waveform of an n-bit counter circuit (n=4) 15. Supposing that the value of the L-column digital video signal input to the m-stage n-bit digital comparator circuit 14 is k, at a point of time when the counter output of Fig. 4 (a) comes to k as shown in Fig. 4 (b), a coincidence pulse Cp is led out from the digital comparator circuit 14.

[0028]

On the other hand, a converting analog input signal Ta supplied from the conversion analog generating circuit 18 is, as shown in Fig. 4 (c), shaped like a waveform changing like a ramp from the white level voltage to the black level voltage. Although the higher voltage side is taken as the black level in the drawing, this is for the liquid crystal element in the normally white mode. In the normally black mode, it will be sufficient that the representations of the black level and the white level are replaced with each other.

[0029]

Accordingly, the coincidence pulse Cp shown in Fig. 4 (b), which is derived from the digital comparator circuit 14, is raised in level to a regulated pulse voltage by the level shifter 16, and then supplied with the converting analog input signal Ta shown in Fig. 4 (c) to the analog switch circuit 17, and the source line output voltage PL of the L- th stage showing the analog voltage value corresponding to the above value of k as shown in Fig. 4 (d) is led out from the analog switch circuit 17. The source line output voltage PL is supplied to the source line 28 of the L-th stage, and applied to the liquid crystal forming the pixel 20 connected to the TFT 30 through the TFT 30 positioned in the intersection of the horizontal line 29 selected by the scan side driver 26. Although the above description deals with the source line of the L- th stage, pixel information corresponding to the input video signal is similarly supplied to the source lines 28 of the first stage to the m-th stage as well.

[0030]

The liquid crystal is AC driven, and in order to perform alternating drive, as shown in Fig. 4 (c), the polarity of a ramp waveform formed by a straight line higher at the right and directing from the white level toward the black level is alternately reversed to form a straight line lower at the right from the black level to the white level alternately. In this case, it is necessary to change the applied voltage of the counter electrode of the liquid crystal depending on the polarity. This is well-known art, so the description is omitted.

[0031]

Generally the characteristic of the voltage applied to the liquid crystal and the transmittance of light is, as described in the above, a curve 50 as shown in Fig. 5. Accordingly, in the range from the black level voltage to the white level voltage shown in Fig. 5, when voltage is linearly applied to the video signal, the optical output contracts near the black and near the while so that the image is inferior in quality and it has no gradation reproducibility. Therefore, in consideration of the curve 50 showing the transmittance characteristic of the liquid crystal, previously an analog video signal and a digital video signal applied to the liquid crystal are corrected to perform the so-called gamma control.

[0032]

In the invention, the above gamma control is performed as follows. That is, as shown in Fig. 6, an analog input signal Ta for conversion led out from the conversion analog signal generating circuit 18 of Fig. 1 is changed to a curve L_2 for performing gamma control on the liquid crystal by a straight line L_1 indicated by a dotted line linearly changing between the white level voltage and the black level voltage, and the thus obtained signal is led out.

[0033]

Fig. 7 is a block diagram of a gamma control circuit, and the gamma control circuit is provided in the conversion analog signal generating circuit 18 of Fig. 1. In Fig. 7, a clock CCLK for the comparator counter led out from the timing generating circuit 11 and a start pulse Sp output in every horizontal period are supplied to an n-bit counter circuit 71. The n-bit counter circuit 71 has the same configuration as the n-bit counter circuit 15 shown in Fig. 1. The counter outputs $Q_0 \ldots Q_n$ (n bit) are led out, and input to the address of the subsequent stage memory 72. The memory 72 is formed of a data table, and the data contents are values corresponding to the correction curve of the gamma control in the order of addresses.

[0034]

Accordingly, the data output of the memory 72 is corrected by the correction curve of the gamma control, and the data output subjected to the gamma control is supplied as the data input of a D-A converter 73. As a result, at the step of a clock CCLK for the comparator counter, the output of the D-A converter 73 changes to generate a conversion analog input signal Ta having the correction curve for the gamma control in one horizontal period. In this case, the step of the clock CCLK for the comparator counter may be the number of steps for gradation, so the circuit itself may be lower speed and more inexpensive as compared with the conventional memories for the gamma control shown in Figs. 10 and 11. The reference numeral 74 is a buffer amplifier, and in the buffer amplifier 74, the voltage regulation of the white level and the black level is performed.

[0035]

Although the above embodiment of the invention deals with monochromatic specification, the same constitution is provided for the respective signals R, G, B of a video signal, and when one pixel is formed by dots of three primary colors R, G, B, it is possible to obtain a driving circuit of a liquid crystal display device for performing color display.

[0036]

[Advantage of the Invention]

The invention has the above constitution, whereby the processing such as holding an analog video signal is not needed, and even in the case of making a high-resolution display increased in number of pixels of one line, the drive of the TFT array can be performed accurately corresponding to an input video signal in a comparatively simple constitution. Further, in the case of converting a digital signal value corresponding to the video signal level to an analog signal to be supplied to the TFT array, the conversion analog input signal is a signal previously corrected according to the gamma control of liquid crystal, so that the gamma control of liquid crystal can be performed in simple constitution to make a display having excellent gradation reproducibility.

[Brief Description of the Drawings]

Fig. 1 is a block diagram of one embodiment according to the invention;

Fig. 2 is a block diagram showing the concrete configuration of the principal part of the invention ;

Fig. 3 is a block diagram showing the concrete configuration of another principal part of the invention ;

Fig. 4 is a diagram explaining the operation of the invention;

Fig. 5 is a diagram showing the transmittance characteristic to the applied voltage of liquid crystal;

Fig. 6 is a diagram explaining the operation of gamma control of liquid crystal ;

Fig. 7 is a block diagram of a gamma control circuit of liquid crystal used in the invention;

Fig. 8 is a block diagram of the prior art;

Fig. 9 is a block diagram of another prior art;

Fig. 10 is a block diagram of a gamma control circuit of liquid crystal in the prior art; and

Fig. 11 is a block diagram of another gamma control circuit of liquid crystal in the prior art.

[Description of the Reference Numerals and Signs]

12: shift register 13: data latch circuit 14: digital comparator circuit 15: n-bit counter circuit 17: analog switch circuit 18: conversion analog signal generating circuit 20: pixel 30: TFT

[FIG. 1]

SVD: DIGITAL VIDEO SIGNAL

11: TIMING GENERATING CIRCUIT

12: M-STAGE N-BIT SHIFT REGISTER

13: M-STAGE N-BIT DATA LATCH

14: M-STAGE N-BIT DIGITAL COMPARATOR

15: N-BIT COUNTER

16: LEVEL SHIFTER

17: ANALOG SWITCH

18: CONVERSION ANALOG SIGNAL GENERATING CIRCUIT

26: SCAN SIDE DRIVER

[FIG. 2]

12: SVD 4-BIT M-STAGE 4-BIT SHIFT REGISTER

13: M-STAGE 4-BIT DATA LATCH

14: M-STAGE 4-BIT DIGITAL COMPARATOR

[FIG. 3]

15: 4-BIT COUNTER

[FIG. 4]

COUNTER OUTPUT K VALUE

DIGITAL COMPARATOR OUTPUT

CP : OUTPUT WHEN THE COUNTER OUTPUT SHOWS THE VALUE OF K.

VOLTAGE

CONVERSION ANALOG INPUT VOLTAGE TA

BLACK LEVEL VOLTAGE

WHITE LEVEL VOLTAGE

VOLTAGE

SOURCE LINE OUTPUT VOLTAGE OF L-TH STAGE

BLACK LEVEL VOLTAGE

ANALOG VOLTAGE SHOWING THE VALUE OF K

WHITE LEVEL VOLTAGE

ONE HORIZONTAL PERIOD

SOURCE LINE OUTPUT CONVERSION PROCESS AT L-TH STAGE WHEN A DIGITAL VIDEO SIGNAL IS THE VALUE OF K.

[FIG. 5]

TRANSMITTANCE CHARACTERISTIC OF LIQUID CRYSTAL

TRANSMITTANCE 100%

VIDEO SIGNAL CORRECTION CURVE

LIQUID VOLTAGE

WHITE LEVEL VOLTAGE BLACK LEVEL VOLTAGE

[FIG. 6]

VOLTAGE

BLACK LEVEL VOLTAGE BLACK LEVEL VOLTAGE

ANALOG CONVERSION SIGNAL WAVEFORM

WHITE LEVEL VOLTAGE WHITE LEVEL VOLTAGE

[FIG. 7]

11: TIMING GENERATING CIRCUIT

71: N-BIT COUNTER → ADDRESS

72: MEMORY → DATA

73: D-A CONVERTER

74: BUFFER AMPLIFIER CONVERSION ANALOG INPUT SIGNAL

WHITE LEVEL, BLACK LEVEL SETTING

[FIG. 8]

PRIOR ART

21: SHIFT REGISTER

22: START PULSE

23: CLOCK

24: ANALOG SWITCH

25: ANALOG VIDEO SIGNAL

26: SCAN SIDE DRIVER

27: POLYSILICON TFT ARRAY EQUIVALENT CIRCUIT

R,G,B: ANALOG VIDEO SIGNAL

1,2,3: A-D CONVERSION

4: DIGITAL VIDEO SIGNAL PROCESSING CIRCUIT

5,6,7: D-A CONVERSION DRIVING ANALOG SIGNAL PROCESSING

PRIOR ART

[FIG. 9]

SVD: DIGITAL VIDEO SIGNAL

26: SCAN SIDE DRIVER

32: M-STAGE N-BIT SHIFT REGISTER

33: M-STAGE N-BIT DATA LATCH

34: M-STAGE N-BIT DIGITAL COMPARATOR - COINCIDENCE PULSE -

35: LEVEL SHIFTER

36: ANALOG SWITCH CIRCUIT

37: ANALOG LATCH CIRCUIT

38: OUTPUT STAGE

39: N-BIT COUNTER

41: CONVERSION ANALOG VOLTAGE

271: A-SI TFT ARRAY

[FIG. 10]

CORRECTION ROM

60, 61, 62: A-D CONVERTER

G DIGITAL VIDEO SIGNAL

B DIGITAL VIDEO SIGNAL

R DIGITAL VIDEO SIGNAL

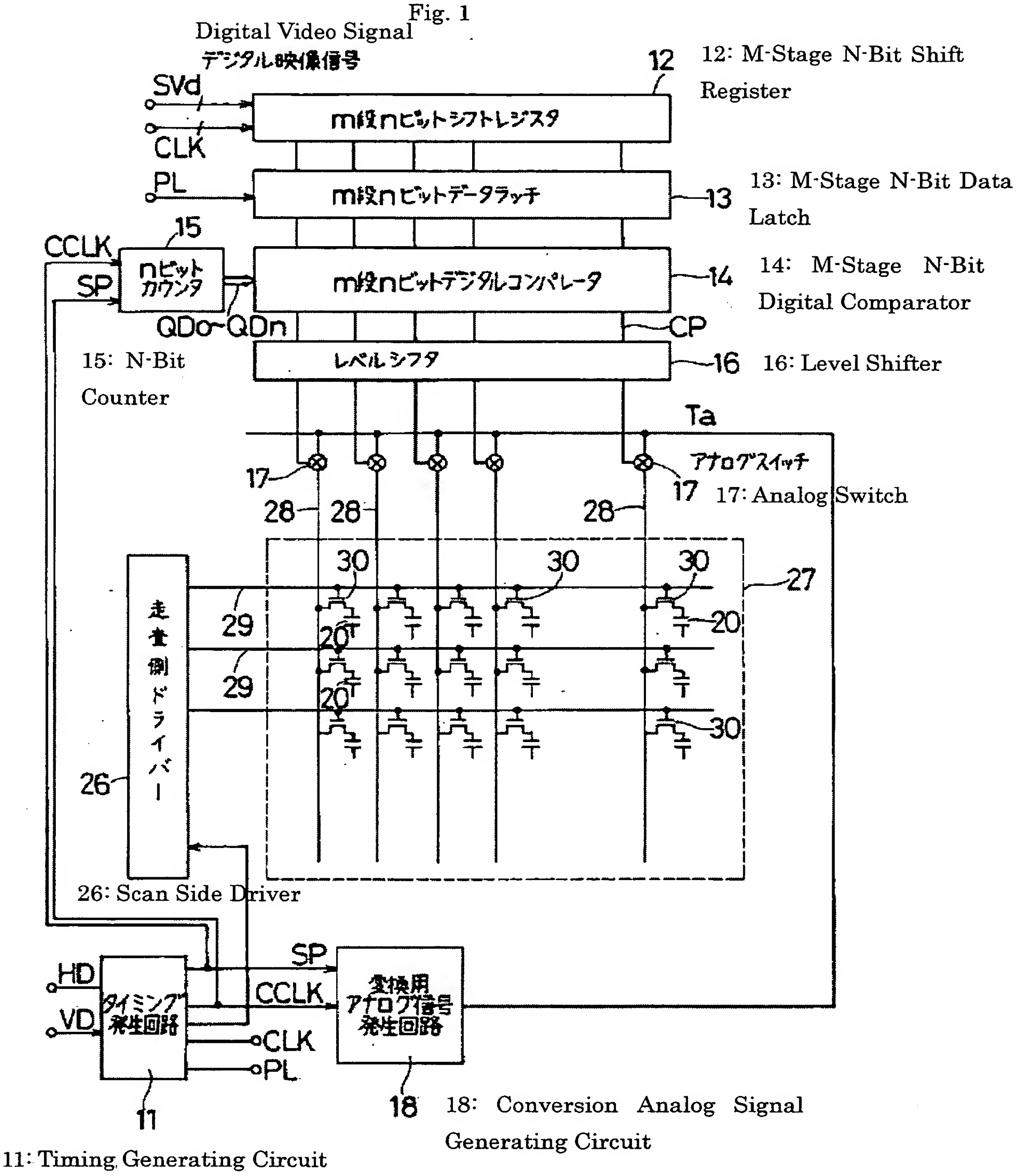
TO LIQUID CRYSTAL SOURCE DRIVER

[FIG. 11]

ANALOG VIDEO SIGNAL

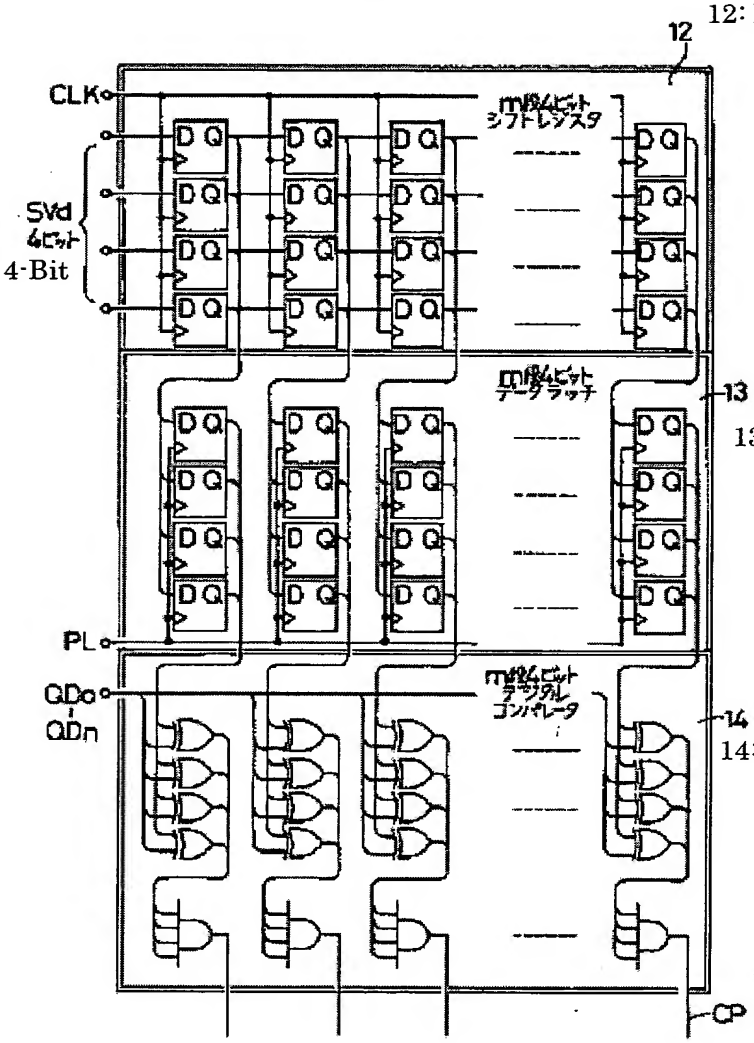
TO LIQUID CRYSTAL SOURCE DRIVER

【図1】
Fig. 1


Digital Video Signal
デジタル映像信号
SVd
CLK
PL
CCLK
SP
12
12: M-Stage N-Bit Shift Register
m段nビットシフトレジスタ
m段nビットデータラッチ
13
13: M-Stage N-Bit Data Latch
15
nビットカウンタ
m段nビットデジタルコンパレータ
14
14: M-Stage N-Bit Digital Comparator
QD0~QDn
CP
15: N-Bit Counter
レベルシフタ
16
16: Level Shifter
Ta
17
アナログスイッチ
17
17: Analog Switch
28
28
28
30
30
30
27
29
20
20
29
20
30
走査側ドライバー
26
26: Scan Side Driver
SP
HD
VD
タイミング発生回路
CCLK
CLK
PL
変換用アナログ信号発生回路
11
18
18: Conversion Analog Signal Generating Circuit
11: Timing Generating Circuit

【図2】
Fig. 2

12: M-Stage 4-Bit Shift Register


12
CLK
SVd
4ビット
4-Bit
m段4ビット
シフトレジスタ
D Q
13
m段4ビット
データラッチ
PL
QDo
QDn
m段4ビット
デジタル
コンパレータ
14
CP

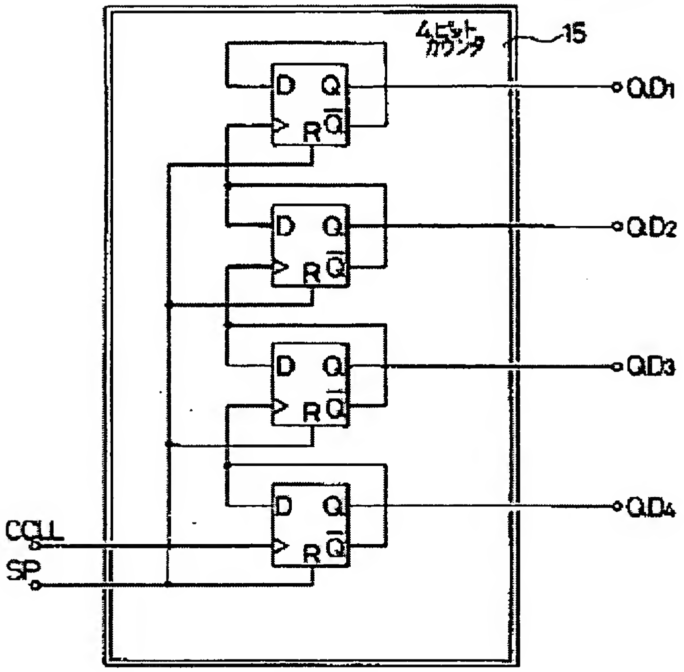
13: M-Stage 4-Bit Data Latch

14: M-Stage 4-Bit Digital Comparator

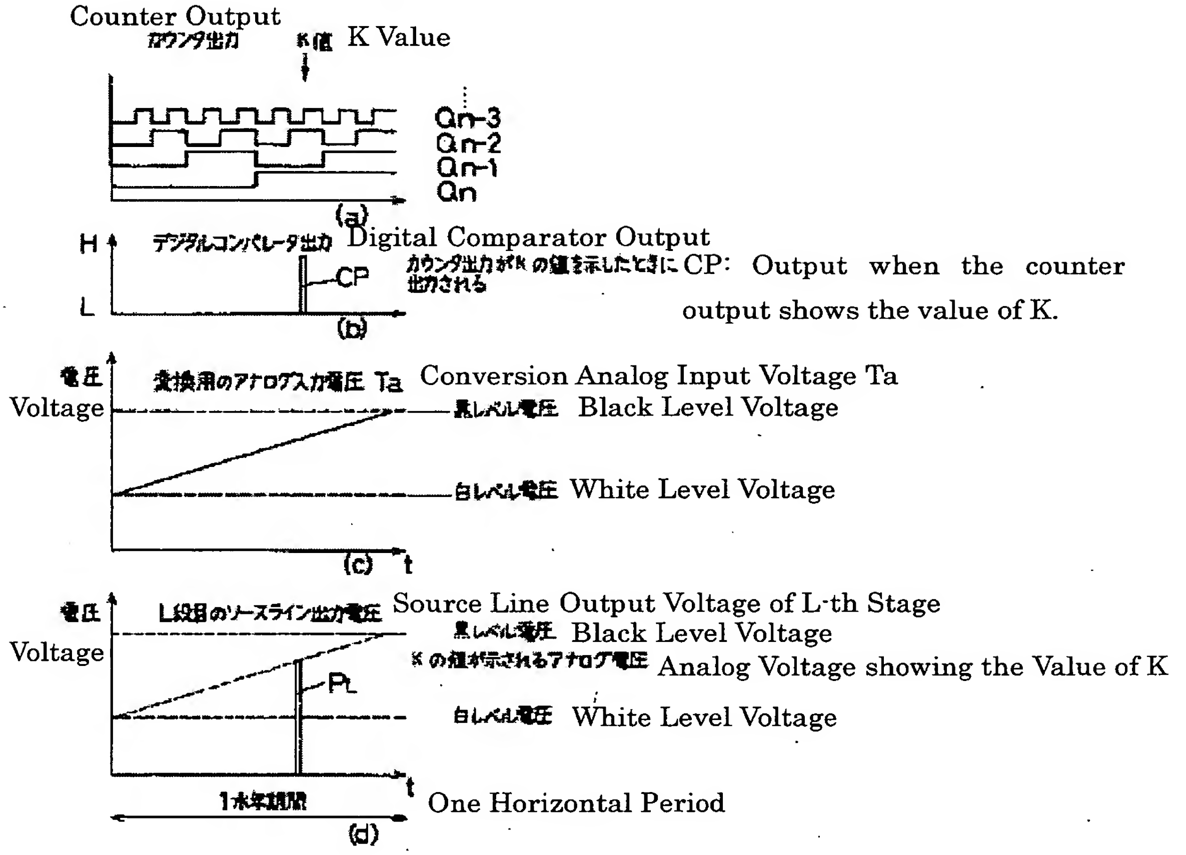
【図3】

Fig. 3

15: 4-Bit Counter


4ビット
カウンタ
15
D
Q
R
$\overline{Q}$
QD1
QD2
QD3
QD4
CCLL
SP

【図4】
Fig. 4

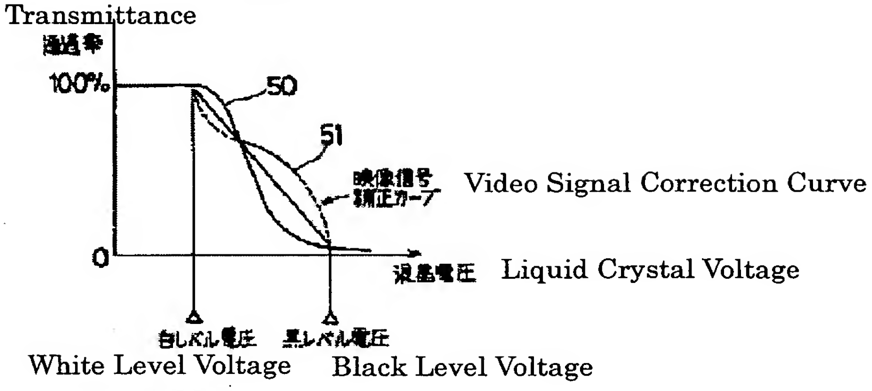

Counter Output
カウンタ出力
K値 K Value
Qn-3
Qn-2
Qn-1
Qn
(a)
H
L
デジタルコンパレータ出力 Digital Comparator Output
CP
カウンタ出力がKの値を示したときに出力される CP: Output when the counter output shows the value of K.
(b)
電圧
Voltage
変換用のアナログ入力電圧 Ta Conversion Analog Input Voltage Ta
黒レベル電圧 Black Level Voltage
白レベル電圧 White Level Voltage
(c)
t
電圧
Voltage
L段目のソースライン出力電圧 Source Line Output Voltage of L-th Stage
黒レベル電圧 Black Level Voltage
Kの値が示されるアナログ電圧 Analog Voltage showing the Value of K
PL
白レベル電圧 White Level Voltage
t
1水平期間 One Horizontal Period
(d)

デジタル映像信号がKの値であるときの
L段目のソースライン出力変換過程

Source Line Output Conversion Process at L-th Stage when a Digital Video Signal is the Value of K.

【図５】

Fig. 5

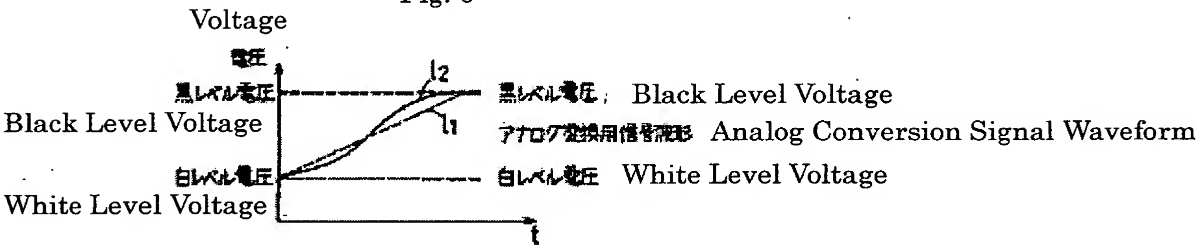


液晶の透過率特性

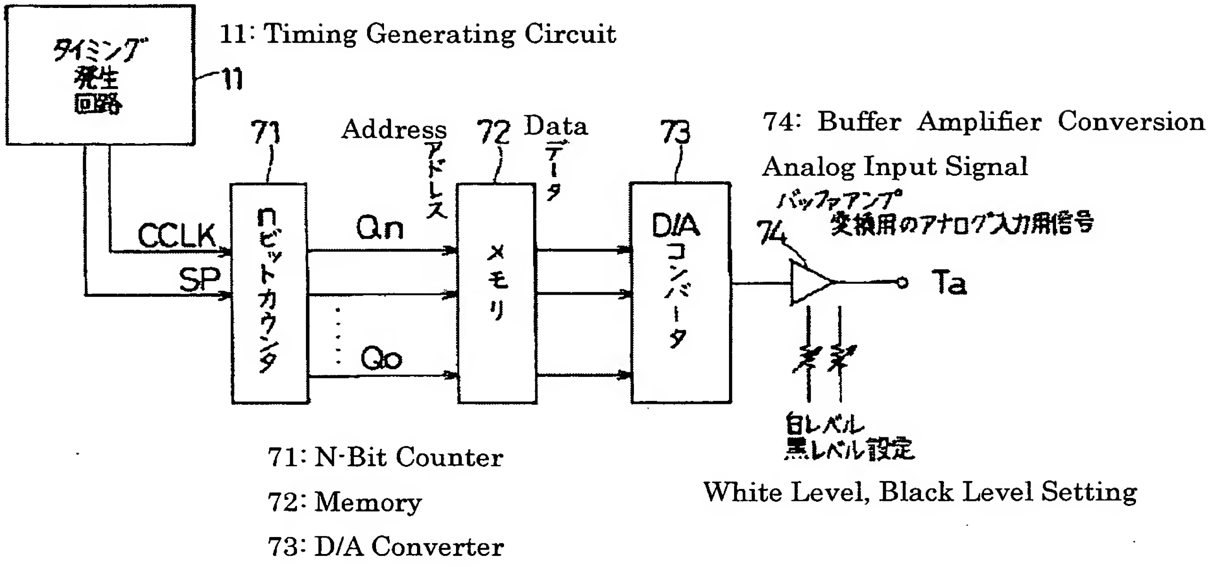
Transmittance Characteristic of Liquid Crystal

【図６】

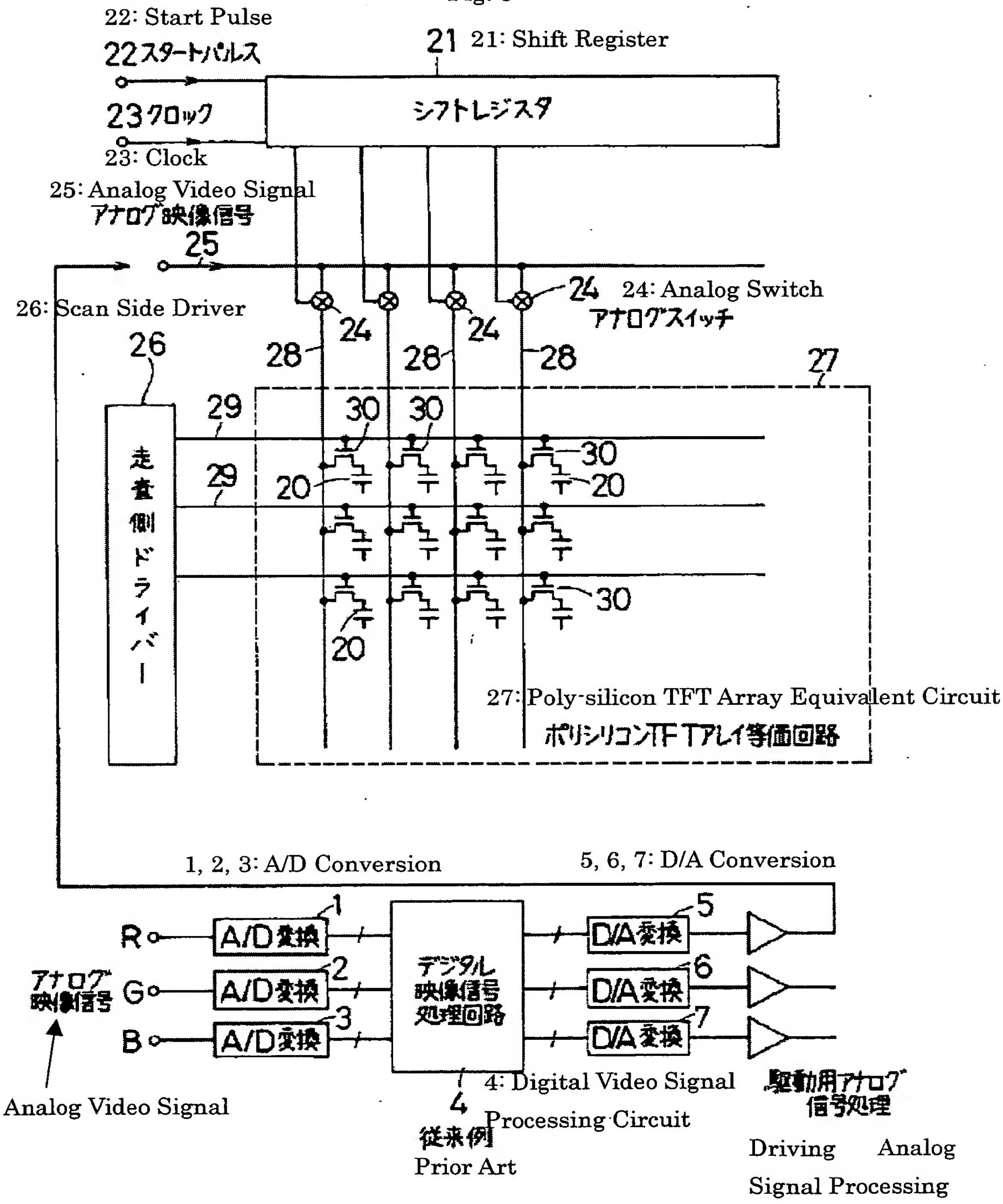
Fig. 6



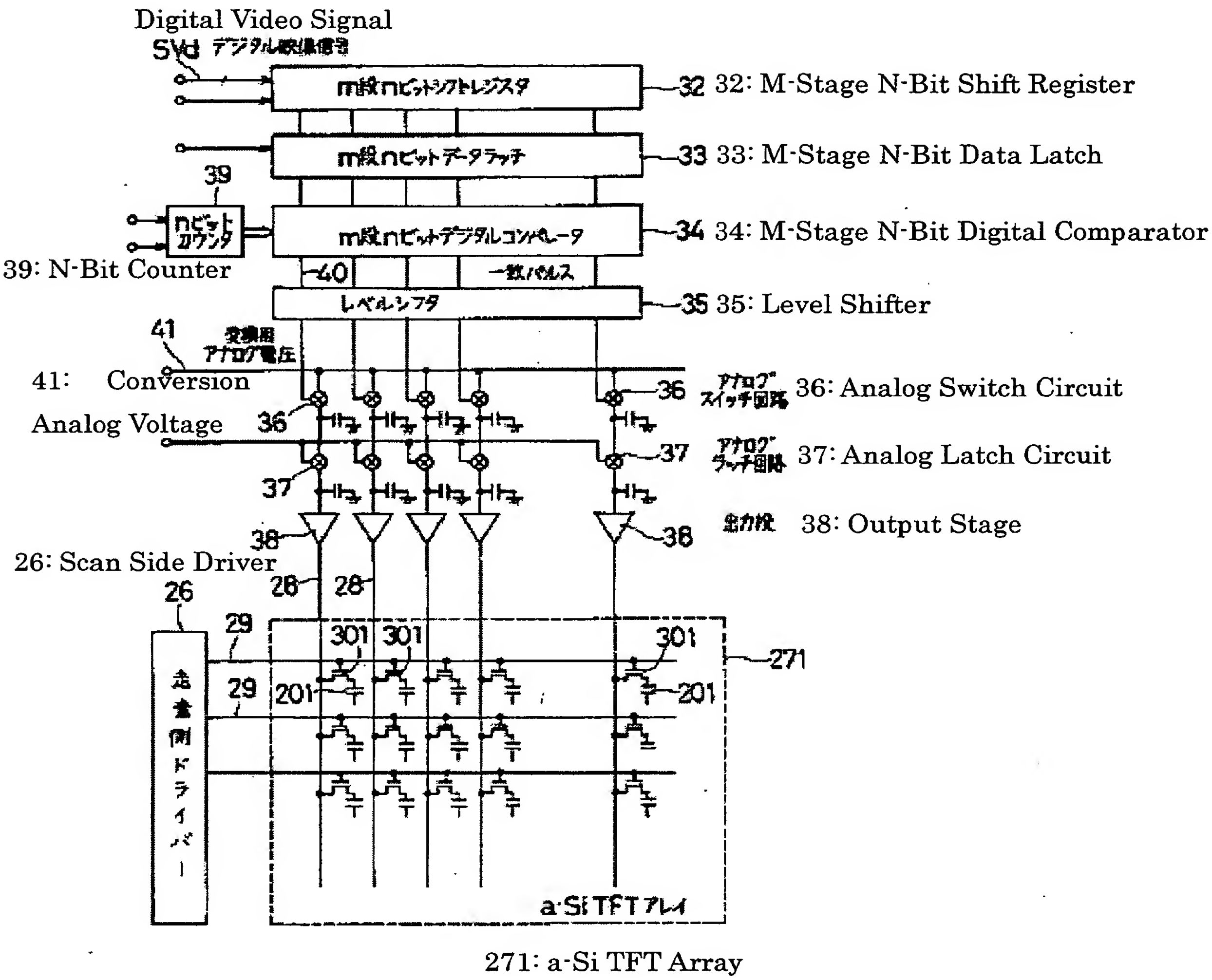
【図７】
Fig. 7


11: Timing Generating Circuit
タイミング発生回路
11
71
Address
アドレス
72
Data
データ
73
74: Buffer Amplifier Conversion Analog Input Signal
バッファアンプ変換用のアナログ入力用信号
CCLK
SP
nビットカウンタ
Qn
Qo
メモリ
D/Aコンバータ
74
Ta
白レベル黒レベル設定
71: N-Bit Counter
72: Memory
73: D/A Converter
White Level, Black Level Setting

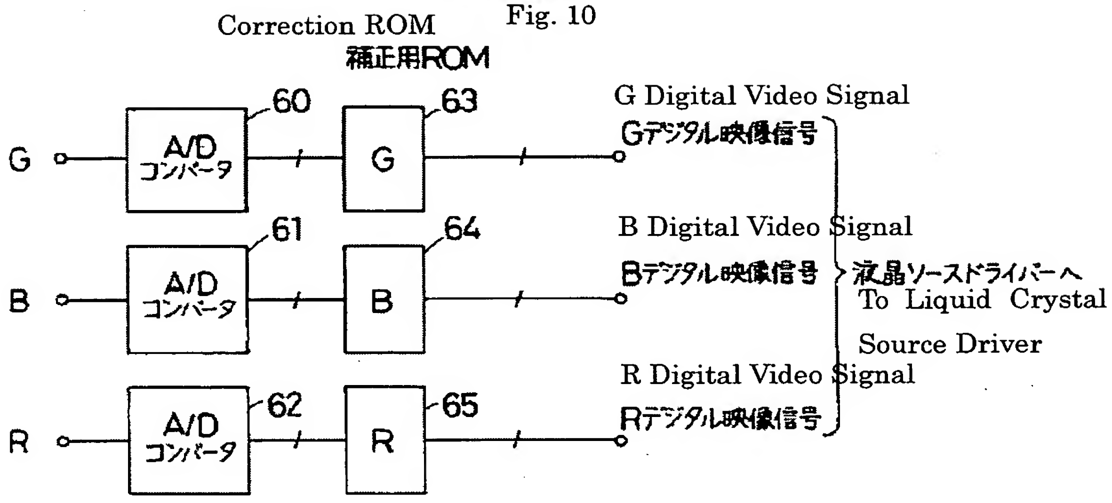
【図８】
Fig. 8


22: Start Pulse
22スタートパルス
23クロック
23: Clock
21
21: Shift Register
シフトレジスタ
25: Analog Video Signal
アナログ映像信号
25
24
24: Analog Switch
アナログスイッチ
26: Scan Side Driver
26
走査側ドライバー
28
28
28
27
29
29
30
30
30
30
20
20
20
27: Poly-silicon TFT Array Equivalent Circuit
ポリシリコンTFTアレイ等価回路
1, 2, 3: A/D Conversion
5, 6, 7: D/A Conversion
R
G
B
A/D変換
A/D変換
A/D変換
1
2
3
デジタル映像信号処理回路
D/A変換
D/A変換
D/A変換
5
6
7
アナログ映像信号
Analog Video Signal
4: Digital Video Signal Processing Circuit
4
従来例
Prior Art
駆動用アナログ信号処理
Driving Analog Signal Processing

【図9】
Fig. 9

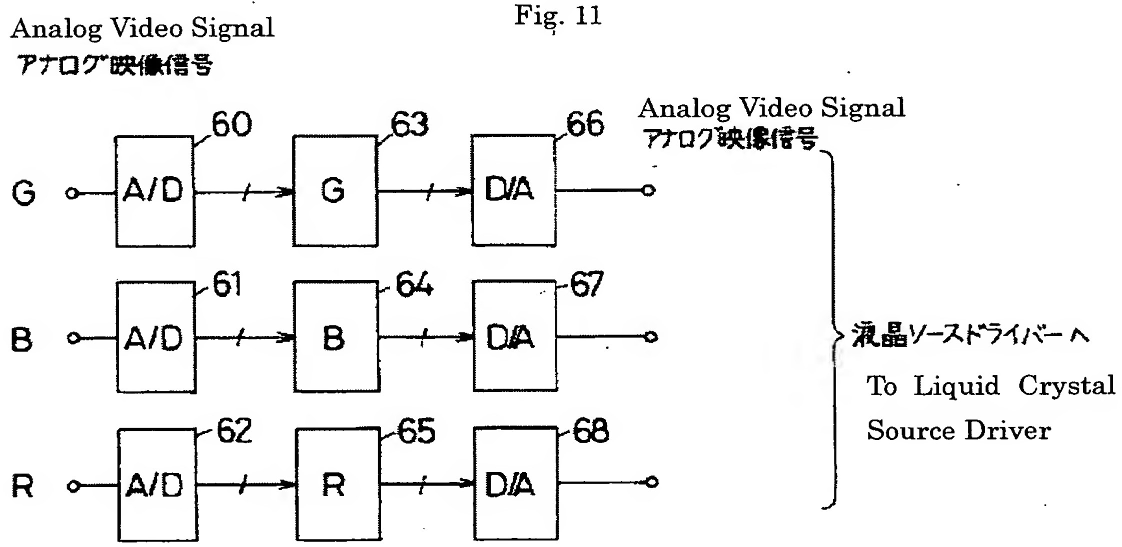

Digital Video Signal
SVd デジタル映像信号
m段nビットシフトレジスタ
32
32: M-Stage N-Bit Shift Register
m段nビットデータラッチ
33
33: M-Stage N-Bit Data Latch
39
nビットカウンタ
m段nビットデジタルコンパレータ
34
34: M-Stage N-Bit Digital Comparator
39: N-Bit Counter
40
一致パルス
レベルシフタ
35
35: Level Shifter
41
変換用アナログ電圧
41: Conversion Analog Voltage
36
アナログスイッチ回路
36: Analog Switch Circuit
37
アナログラッチ回路
37: Analog Latch Circuit
38
出力段
38: Output Stage
26: Scan Side Driver
26
28
29
301
201
271
走査側ドライバー
a-Si TFTアレイ
271: a-Si TFT Array

【図１０】
Fig. 10


Correction ROM
補正用ROM
60
63
G
A/D
コンバータ
G
G Digital Video Signal
Gデジタル映像信号
61
64
B
A/D
コンバータ
B
B Digital Video Signal
Bデジタル映像信号
液晶ソースドライバーへ
To Liquid Crystal Source Driver
62
65
R
A/D
コンバータ
R
R Digital Video Signal
Rデジタル映像信号

60, 61, 62: A/D Converter

【図１１】
Fig. 11


Analog Video Signal
アナログ映像信号
60
63
66
Analog Video Signal
アナログ映像信号
G
A/D
G
D/A
61
64
67
B
A/D
B
D/A
液晶ソースドライバーへ
To Liquid Crystal Source Driver
62
65
68
R
A/D
R
D/A